D1 cont.

film or an organic resist film as the etching mask. Since GaAs substrates are readily processed either mechanically or chemically as mentioned above, high-frequency operation and high-power output of GaAs FETs have already been realized by thinning the substrate and making the via hole in the substrate.

Page 4, please replace the first full paragraph, continuing to page 5, with the following new paragraph:

D2

However, it is difficult to employ the technique successfully used in GaAs FETs for thinning the substrate and making the via hole in the substrate also for fabrication of GaN FETs. As referred to above, sapphire substrates are often used for manufacturing GaN FETs. Sapphire, however, is much harder than GaAs, and it is extremely difficult to reduce the thickness of the sapphire substrate by using the above-explained conventional lapping technology. If it is forcibly thinned by lapping, it will form a large curve due to a lapping strain to be concave on the major surface side where the device should be made, and it will finally break down. Also regarding the via hole to be made in the sapphire substrate, since sapphire is very stable in chemical property, wet etching cannot be used without an effective etchant. As to dry etching by RIE, since its etching rate is as very low as several μm/hr in maximum, and there is no etching mask being selectively acceptable for selective etching. Therefore, it is actually impossible to made the via hole with any of these methods. So, when making GaN FET on a sapphire substrate, it has been difficult to realize high-frequency operation and high-power output relying on thinning the substrate and making the via hole.

Page 7, please replace the second full paragraph with the following new paragraph:

D3

The present invention as summarized below, goes toward overcoming the above-indicated problems involved in the conventional techniques.

Page 7, please replace the third full paragraph, continuing to page 8, with the following new paragraph:

For thinning a sapphire substrate already having formed a device using GaN semiconductors, there are some problems to solve. One of the problems is to thin the substrate sufficiently, namely to a thickness around 100 μm, for example, tens or μm, in the process of thinning the sapphire substrate by using lapping or some other method, without damaging the device on the surface of the substrate, while minimizing the processing strain and preventing warpage or breakage of the substrate. When using a sapphire substrate, unlike the case using a GaAs substrate, warpage causes difficulties in subsequent processes unless substantially all of the strain in the thinned substrate is removed finally. Another problem is to find out an optimum processing method for making the via hole in any desired location of the sapphire substrate. Use of molten coral sand around 900 °C and use of molten phosphoric acid around 400 °C are known as methods for wet etching of sapphire. The present invention estimates the applicability of these methods as a technique for making the via hole in a sapphire substrate and also to find out possible materials usable as an etching mask in the technique. The present invention also discloses a new simple method for making the via hole without using the etching mask.

Page 10, please replace the first full paragraph, continuing to page 11, and to page 12, with the following new paragraph:

For making the via hole, dry etching such as conventional RIE cannot be employed. Then, consideration is made on using the following method. That is, as shown in Fig. 2, for example, after growing a GaN semiconductor layer 2 with a thickness of several μm in total, for example, on the surface of a sapphire substrate 1, and a GaN FET 3 is formed on the GaN semiconductor layer 2. After that, a

metal wiring and a pad for the GaN FET 3 are made. Reference numeral 4 denotes a Au pad electrically connected to the source of the GaN FET 3. Thereafter, an inter-layer insulating film 5 such as SiO_2 film is formed on the GaN semiconductor layer 2 to cover the Au pad 4. Subsequently, the sapphire substrate 1 is thinned to a thickness of 100 μm or less, for example to a thickness around tens of μm. After that, the bottom surface of the sapphire substrate 1 is covered locally at the location for the via hole by a multi-layered etching mask 6 made by stacking metal thin films. Used as the multi-layered film is, for example, a two-layered film stacking a thin film of a metal resistant to phosphoric acid, such as Pt, Au, Pd, or the like, on a thin film of a metal well [adhesive] adherent to the sapphire substrate, such as Ni, Cr, Ti, or the like. On the other hand, a protective film of polyimide 7, for example, is formed on the surface of the inter-layer insulating film 5. Thereafter, the bottom surface side of the sapphire substrate 1 is immersed into an etchant of phosphoric/sulfuric acid solution held at approximately 280 °C, for example, to etch it. In this case, since the etching rate is approximately 10 μm/hr, the etching time is adjusted depending upon the thickness of the sapphire substrate 1. In this manner, as shown in Fig. 3, the via hole 8 is made in the sapphire substrate 1. Then, next using RIE, part of the GaN semiconductor layer 2 exposed at the bottom of the via hole 8 is removed by etching to expose the Au pad 4 there. In the process of etching the GaN semiconductor layer 2, if Cl_2 gas is sued as the etching gas, since the etching rate is 5 to 10 μm/hr and the ratio of the etching rate for Au is approximately 3 or more, a sufficient thickness of the Au pad 4 can be maintained even after etching the GaN semiconductor layer to a slightly over-etching level, if the Au pad 4 originally has a thickness around 1 μm or more. It may occur that the etching mask 6 on the bottom surface of the sapphire substrate 1 is removed while the GaN semiconductor layer 2 is etched by RIE. However, it is immaterial.

Page 19, please replace the fourth full paragraph with the following new paragraph:

In the present invention, each nitride III-V compound semiconductor includes at least Ga and N, and may additionally include one or more group III elements selected from the group consisting of Al, In and B and/or one or more group V elements selected from the group consisting of As and P. Some specific examples of nitride III-V compound semiconductors are GaN, AlGaN, GaInN and AlGaInN.

Page 28, please replace the first full paragraph with the following new paragraph:

Next as shown in Fig. 11, here again, by vacuum evaporation, for example, a 20 nm thick Cr film and a 5 μm thick Au film, for example, are sequentially stacked to form a Cr/Au film 36. Thereafter, a Au film 37 having a thickness as sufficiently thick as approximately 100 μm, for example, is made on the Cr/Au film 36 by plating, for example. Then, the protective film 26 of polyimide is removed by an organic solvent.

IN THE CLAIMS:

Please enter the following amended claims:

9. (Amended) A semiconductor device comprising:

a single-crystal substrate made of a material different from nitride III-V compound semiconductors, and

a device formed on one major surface of said single-crystal substrate by using III-V compound semiconductors,

wherein electrical connection to said device is made through a via hole formed in said single-crystal substrate.

10. (Amended) The semiconductor device according to claim 9, wherein said single-crystal